DOCUMENT-IDENTIFIER: US 20010044205 A1

TITLE: Method of planarizing a conductive plug situated under a ferroelectric capacitor

--------- KWIC ---------

[0033] Basically, gate structures 106 include a gate dielectric (preferably comprised of silicon dioxide, an oxynitride, a silicon nitride, BST, PZT, a silicate, any other high-k material, or any combination or stack thereof, a gate electrode (preferably comprised of polycrystalline silicon doped either p-type or n-type with a silicide formed on top or a metal such as titanium, tungsten, TiN, tantalum, TaN or a metal), and side wall insulators (preferably comprised of an oxide, a nitride, an oxynitride, or a combination or stack thereof). In general the generic terms oxide, nitride and oxynitride refer to silicon oxide, silicon nitride and silicon oxy-nitride. The term "oxide" may, in general, include doped oxides as well such as boron and/or phosphorous doped silicon oxide. Source/drain regions 108 are preferably implanted using conventional dopants and processing conditions. Lightly doped drain extensions as well as pocket implants may also be utilized. In addition, the source/drain regions 108 may be silicided (preferably with titanium, cobalt, nickel, tungsten or other conventional silicide material).

remove residual (EtCp).sub.2 Ru from the gas phase. After that, water vapor, which was evaporated from an external source bottle, was introduced into the reaction chamber and contacted for 2.0 s with the substrate surface, where H.sub.2 O molecules reacted with adsorbed Ru compound molecules. Then the reaction chamber was purged with inert nitrogen gas to remove residual H.sub.2 O and reaction by-products. The set of pulses was repeated until a ruthenium oxide thin film with the desired thickness was grown on the substrate. Optionally some amount of oxygen gas may be added to the H.sub.2 O flow to control the oxidation state of Ru. Relatively mild oxidizing agents were used. Strong oxidizing agents, e.g. ozone, have a tendency to oxidize part of the adsorbed ruthenium into its maximum oxidation state +8 and the resulting RuO.sub.4 is highly volatile and thus the growth of RuO.sub.2 is disturbed because of desorbing RuO.sub.4.

Detailed Description Paragraph Equation - DEEQ (3):

2(--RuF.sub.3)(ads.)+4H.sub.2 O(g).fwdarw.2[--RuO (--OH)](ads.)+6HF(g) (V)

Other Reference Publication - OREF (8):

Campbell, S.A. et al., "Titanium dioxide (TIO.sub.2)-based gate insulators, "IBM J. Res. Develop.Vol. 43, No. 3, pp. 383-392. (May 1999).

word lines and on opposite sides of the drain region. The word lines 105 act as gate electrodes, and the drain and source regions are doped with N-type dopants.

Detailed Description Text - DETX (9):

Referring now to FIG. 3, a gate insulation layer 102 is formed on a P-type semiconductor substrate 100 in which an active region and an inactive region are defined by an isolation layer 101. A first conductive sublayer 103 and a second conductive sublayer 104 are sequentially formed to form an electrode layer. The first conductive layer 103 may comprise a polysilicon layer doped with impurities, and the second conductive layer 104 may comprise at least one of platinum (Pt), iridium (Ir), ruthenium (Ru), tungsten (W), iridium oxide (Ir.sub.2 O.sub.3), rhenium oxide (ReO.sub.2) and ruthenium oxide (RuO.sub.2).

Detailed Description Text - DETX (10):

Referring to FIG. 4, the electrode layer comprised of the first and second conductive sublayers 103 and 104, and the gate insulation film 102 are patterned to form a gate electrode 105 in the active region of the semiconductor substrate 100, and a lower capacitor electrode 108 in the inactive region, which extends parallel to the gate electrode 105. The lower electrode 108 also forms a plate line.

to three times the thickness of the layer 14 and have a mean closest distance that is at least two times the thickness of the layer 14.

Detail Description Paragraph - DETX (15):

[0033] The remaining ruthenium oxide zones 16 shown in FIG. 3 constitute, together with the underlying conductive layer 12, an enhanced-surface-area conductive layer compatible with high-dielectric-constant dielectric materials. To form a capacitor with the enhanced-surface-area conductive layer of FIG. 3, a layer 24 of a dielectric material is provided on the structure. The layer 24 may be of a high-dielectric-constant dielectric material, generally any dielectric with a dielectric constant of at least 9, or more preferably, a dielectric constant of at least 20, with tantalum pentoxide (Ta.sub.2O.sub.5) being a specific example. The dielectric material may be formed conformally over the enhanced-surface-area conductive layer, as shown in FIG. 4. Other high-constant dielectrics may also be employed, such as barium strontium titanium oxide, lead zirconium titanium oxide, and strontium bismuth tantalum oxide, for example. Because of the relatively large diameter of the previously removed ruthenium phase zones, the layer 24 can conform somewhat to the shape

of the enhanced-surface-area conductive layer, allowing an enhanced surface area on both sides of the layer 24. In other words, the surface of the layer 24 away from the remaining ruthenium oxide zones is desirably not flat, but follows at least somewhat the contours of the underlying ruthenium oxide, providing an enhanced surface area on this surface as well

Detail Description Paragraph - DETX (4):

[0020] FIG. 3 depicts the next step in the FEM cell construction, that being the deposition of a lower polycrystalline silicon ("polysilicon") layer 22 over the gate oxide 20. After being deposited to a preferred thickness of about 500 to 700 .ANG., the lower polysilicon layer 22 is doped to the desired polarity, which preferably is n-type. The lower polysilicon layer 22 assists in protecting the gate oxide 20 from damage during further process steps.

Detail Description Paragraph - DETX (5):

[0021] Formation of a FEM gate unit is begun atop the polysilicon layer 22 by depositing a bottom electrode 26. The bottom electrode 26 is deposited by known deposition processes, such as physical vapor deposition ("PVD") or chemical vapor deposition ("CVD"), and preferably comprises platinum. Alternatively, other materials that may be used to form the bottom electrode 26 include ruthenium, iridium, RuO, or IrO.sub.2, or other suitable noble metal oxides or alloys thereof. The thickness of the electrode 26 is from about 500 to 1,500 .ANG.. It is noted that, in an alternative embodiment, the lower polysilicon layer 22 may be eliminated from the FEM cell. In such an embodiment, the bottom electrode 26 would provide the protective function for the gate oxide 20 formerly provided by the lower polysilicon layer 22 as noted above.

starting materials. After spin coating the mixed solution, the film is dried at 150.degree. C., and temporary baking of 400.degree. C., 30 minutes is performed at dry air atmosphere. After this is repeated five times, thermal treatment of 500.degree. C., one minute in atmosphere of O.sub.2 is performed as shown in FIG. 5C. Thus, a ferroelectric substance film 16 of 250 nm is formed. Here, the PZT film is formed placing 0.52 for x in PbZr.sub.xTi.sub.1-xO.sub.3 (PZT(52/48), hereinafter).

Detail Description Paragraph - DETX (30):

[0071] Further, an iridium layer and an iridium oxide layer are formed on the ferroelectric substance film 16 by spattering so as to form a control gate 17. Here, the iridium layer and the iridium oxide layer are formed so as to be 200 nm thickness in all.

Detail Description Paragraph - DETX (32):

[0073] After that, by injecting boron (B) ion masking the gate electrode pattern, source-drain regions 2 and 3 of p-type diffusion layer as shown in FIG. 5E.

Detail Description Paragraph - DETX (34):

DOCUMENT-IDENTIFIER: US 20020072223 A1

TITLE: Method of enhancing adhesion of a conductive barrier layer to an underlying conductive plug and contact for ferroelectric applications

---------- KWIC ---------

[0032] Basically, gate structures 106 include a gate dielectric (preferably comprised of silicon dioxide, an oxynitride, a silicon nitride, BST, PZT, a silicate, any other high-k material, or any combination or stack thereof), a gate electrode (preferably comprised of polycrystalline silicon doped either p-type or n-type with a silicide formed on top or a metal such as titanium, tungsten, TiN, tantalum, TaN or a metal), and side wall insulators (preferably comprised of an oxide, a nitride, an oxynitride, or a combination or stack thereof). In general the generic terms oxide, nitride and oxynitride refer to silicon oxide, silicon nitride and silicon oxy-nitride The term "oxide" may, in general, include doped oxides as well such as boron and/or phosphorous doped silicon oxide. Source/drain regions 108 are preferably implanted using conventional dopants and processing conditions. Lightly doped drain extensions as well as pocket implants may also be utilized. In addition, the source/drain regions 108 may be silicided (preferably with titanium, cobalt, nickel, tungsten or other conventional silicide material).

[0005] It would also be useful to have a high dielectric constant capacitor that can be used generally in integrated circuits, such as for gate dielectric films in metal-oxide-semiconductor field effect transistors (MOSFETs), ferroelectric field effect transistors (ferroelectric FETs), and other transistors, as buffer layers to prevent unwanted interactions between certain materials, as diffusion barriers to prevent diffusion of elements from one layer to another, and as interlayer dielectrics. In each of these applications it is useful that the material have electronic values that do not change with temperature and voltage. In addition, each of these applications have additional electronic requirements. It is particularly difficult to predict if a high dielectric material will be effective in gate insulator films in MOSFETs, ferroelectric FETs, and other transistors because, in this application, it must meet multiple, often conflicting, requirements. In addition to having a capacitance that is flat with respect to temperature, voltage and thickness variations, they must have low leakage current and a high breakdown voltage, they must not alter the threshold voltage of the transistor as a function of gate voltage, and they must be an effective barrier against charge injection. Buffer layers must be compatible with both the material they buffer and the surrounding integrated circuit materials. Diffusion barriers must be effective in preventing migration of particular elements at elevated temperatures and must not themselves include elements that can migrate. Interlayer dielectrics must have low leakage currents and have a high breakdown voltage. As integrated circuits become smaller, all the above requirements become more and more stringent, since thicknesses of the materials decrease and the distances between dissimilar materials shrink. The paucity of materials

electrically connected to the drain region and extending along the integrated circuit substrate orthogonal to the word lines. In preferred embodiments of the invention, a first conductive layer is included, and the pair of spaced apart word lines and the lower electrodes comprise first and second portions respectively of the first conductive layer. The first conductive layer more preferably comprises a first sublayer including doped polysilicon and a second sublayer on the first sublayer. The second sublayer preferably comprises at least one of platinum, iridium, ruthenium, tungsten iridium oxide, rhenium oxide and ruthenium oxide .

Summary of Invention Paragraph - BSTX (27):

[0025] A sidewall spacer may be provided on the ferroelectric layer sidewall that reduces diffusion from the ferroelectric layer. The sidewall spacer preferably comprises aluminum oxide. A capping layer is also preferably provided on the upper electrode opposite the ferroelectric layer, to reduce diffusion from the ferroelectric layer through the upper electrode. The capping layer preferably comprises titanium oxide . The ferroelectric layer preferably comprises at least one of PZT, PLZT and Yi, and the upper electrode preferably comprises the same material as the second sublayer. Accordingly, integrated circuit ferroelectric memory device fabrication methods and structures are provided that can use fewer conductive layers and/or masking steps to allow high density, improved reliability and/or reduced costs.

DOCUMENT-IDENTIFIER: US 20020063299 A1

TITLE: Semiconductor device and manufacturing method

--------- KWIC ---------

[0052] Hereinafter, when both a post-gate oxide film (including an oxide film on the source/drain region) and a liner layer are provided, they are collectively referred to as the first side wall film and the silicon nitride film 5 at the side of the gate electrode is referred to as the second side wall film. When still another film is formed beside the silicon nitride film, these films are collectively referred to as the second side wall film. It should be noted that the second side wall film is not limited to a silicon nitride film and the silicon substrate may contain Ge. The gate insulating film may be a silicon oxide film, a silicon nitride film, a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element.

US006452229B1

(12) **United States Patent**
Krivokapic

(10) **Patent No.: US 6,452,229 B1**
(45) **Date of Patent: Sep. 17, 2002**

(54) **ULTRA-THIN FULLY DEPLETED SOI DEVICE WITH T-SHAPED GATE AND METHOD OF FABRICATION**

(75) Inventor: **Zoran Krivokapic**, Santa Clara, CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/081,104**

(22) Filed: **Feb. 21, 2002**

(51) **Int. Cl.**[7] **H01L 29/76**; H01L 29/94; H01L 27/01; H01L 27/12; H01L 31/0392

(52) **U.S. Cl.** **257/330**; 257/332; 257/347

(58) **Field of Search** 257/330, 332, 257/346, 347, 401, 411

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,567,966	A	* 10/1996	Hwang	257/347
6,013,553	A	1/2000	Wallace et al.	
6,020,024	A	2/2000	Maiti et al.	
6,060,749	A	* 5/2000	Wu	257/347
6,100,204	A	8/2000	Gardner et al.	
6,127,699	A	* 10/2000	Ni et al.	257/330

* cited by examiner

Primary Examiner—Ngân V. Ngô
(74) *Attorney, Agent, or Firm*—Renner, Otto, Boisselle & Sklar, LLP

(57) **ABSTRACT**

A fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET) and methods of formation. The FET includes a T-shaped gate formed at least in part in a recess formed in a layer of semiconductor material and over a body region that is disposed between a source and a drain. The gate includes a gate electrode spaced apart from the body by a gate dielectric made from a high-K material.

13 Claims, 5 Drawing Sheets

Date

(12) **United States Patent**
Krivokapic

(10) **Patent No.: US 6,509,234 B1**
(45) **Date of Patent: Jan. 21, 2003**

(54) **METHOD OF FABRICATING AN ULTRA-THIN FULLY DEPLETED SOI DEVICE WITH T-SHAPED GATE**

(75) Inventor: **Zoran Krivokapic**, Santa Clara, CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/200,652**

(22) Filed: **Jul. 22, 2002**

Related U.S. Application Data

(62) Division of application No. 10/081,104, filed on Feb. 21, 2002, now Pat. No. 6,452,229.

(51) **Int. Cl.**[7] **H01L 21/336**; H01L 21/00; H01L 21/28

(52) **U.S. Cl.** **438/270**; 438/297; 438/303; 438/151; 438/572; 438/574; 438/576; 438/580

(58) **Field of Search** 438/149, 151, 438/270, 297, 303, 572, 574, 575, 576, 579, 580, 581, 58

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,358,885	A	*	10/1994	Oku et al.
5,552,620	A	*	9/1996	Lu et al.
5,567,966	A		10/1996	Hwang
6,013,553	A		1/2000	Wallace et al.
6,020,024	A		5/2000	Wu
6,060,749	A		5/2000	Wu
6,100,204	A		8/2000	Gardner et al.
6,127,216	A	*	10/2000	Yu
6,127,699	A	*	10/2000	Ni et al.
6,159,781	A	*	12/2000	Pan et al.
6,333,229	B1	*	12/2001	Furukawa et al.
6,348,385	B1	*	2/2002	Cha et al.
6,452,229	B1	*	9/2002	Krivokapic

* cited by examiner

Primary Examiner—John F. Niebling
Assistant Examiner—Stanetta Isaac
(74) *Attorney, Agent, or Firm*—Renner, Otto, Boisselle & Sklar, LLP

(57) **ABSTRACT**

A method of forming a fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET). The method includes forming a T-shaped gate electrode formed at least in part in a recess formed in a layer of semiconductor material and over a body region that is disposed between a source and a drain. The method includes spacing the gate electrode from the body by a gate dielectric made from a high-K material.

15 Claims, 5 Drawing Sheets